Abstract

A non-complementary comparator includes an evaluation element such as a memory cell, a differential amplifier, or another type of circuit capable adapted to perform an evaluation function, and at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element. The first and second input legs have non-complementary structures relative to one another, with each of the non-complementary structures having associated therewith a variable parameter, e.g., a variable resistance, variable current or variable voltage, having a value that is a function of a corresponding input signal. The evaluation element performs a comparison of at least first and second inputs applied to the respective first and second input legs. The input legs may each be implemented as a weighted array of transistors, with each of the transistors in the weighted array associated with a given leg corresponding to a particular bit or other portion of an input signal applied to that leg. The non-complementary comparator may be used as a multi-digit comparator to determine the relative weight of digital words, or to implement other comparator circuits such as, e.g., majority rule circuits, analog common mode comparators, greater than/less than circuits, array addition and comparison circuits, serial adder-binary search (SA-BS) circuits, analog adders, add-compare-select (ACS) circuits, coupled memory cell comparators, and comparators with mask functions.